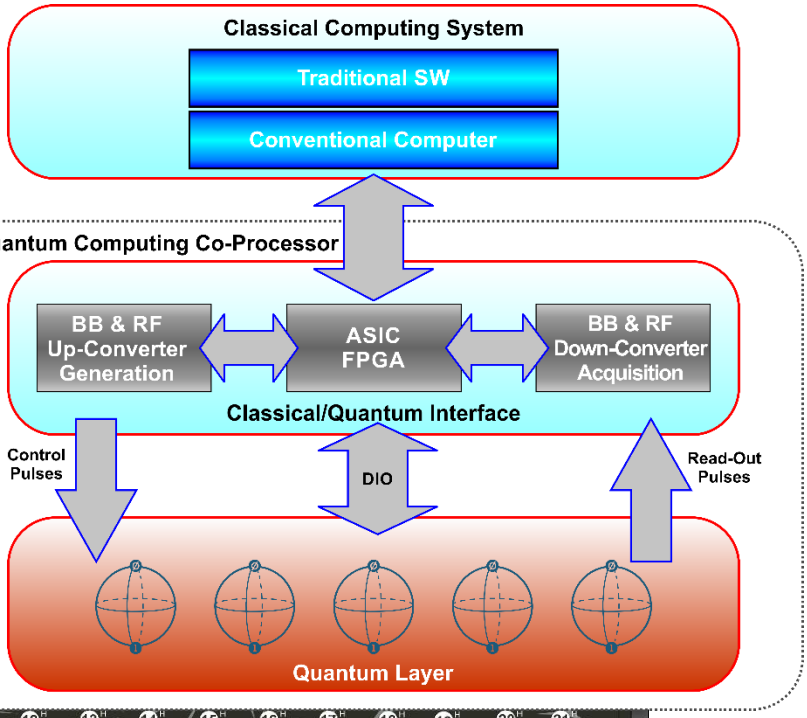
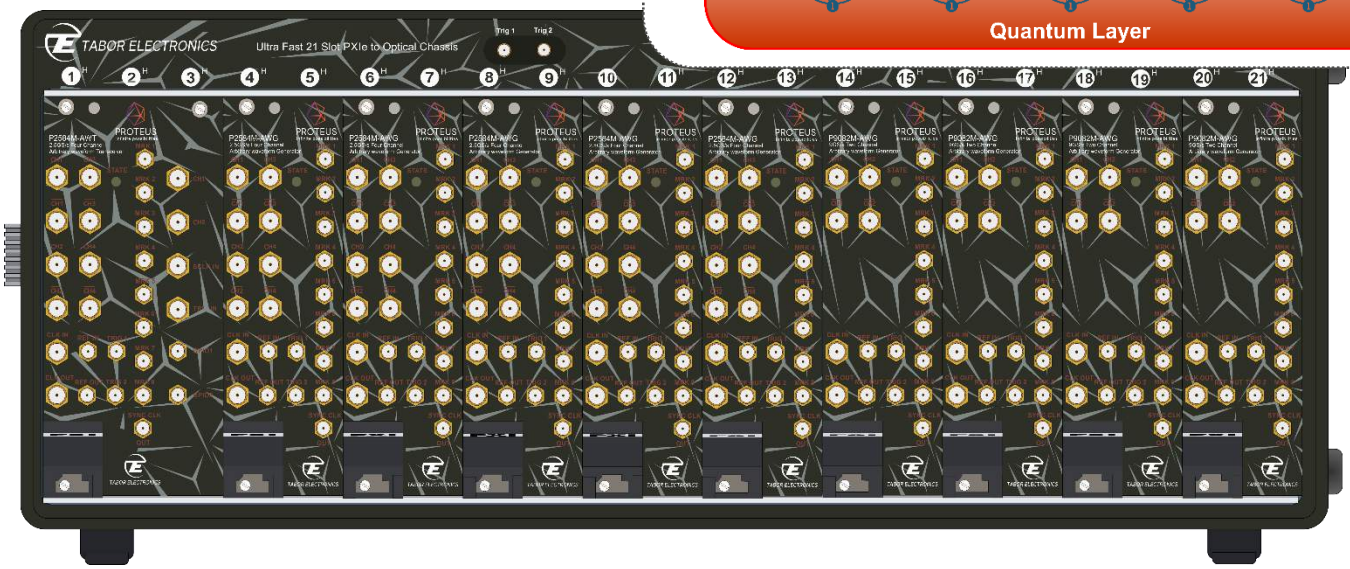
Direct to Microwave

New trends in RF/μW signal generation and acquisition and real-time closed-loop control for classical to quantum computer interfacing

PROTEUS
Infinite possibilities





Simulate, Stimulate, Test...

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From the “proof of concept” experiment to the fully functional quantum computer

In the past, most experiments related with quantum computing did not have the goal of performing actual computations. They were basically “proof-of-concept” experiments applied to the research of materials and architectures for Qubits and the best way to control and capture their quantum state, implement quantum gates, and validate their operational principles. The qubit control devices of choice to implement such research systems were traditional, high-performance, T&M lab equipment controlled from a classical computer through established communication interfaces and control protocols (fig. 1). Several AWGs (Arbitrary Waveform Generators) to produce the quantum state control and reading signals combined with some digitizers or real-time DSOs (Digital Storage Oscilloscope) to establish the state of the qubits, were the foundation of these research systems. Most AWGs and digitizers cannot cope with the frequencies of the control and state-readout signals. Those typically consists in some sort of microwave carrier modulated by some sequence of near-gaussian pulses in amplitude and phase (figure 2). Instead of directly generating or capturing such signals, AWGs and DSOs must be combined with some mixers, IQ modulators, amplifiers and filters (figure 3). Mixers and IQ modulators require additional microwave L.O. generators (i.e. CW microwave generators). Additional control signals, analog and digital, are also required. As a result, the cost per qubit was high while the scalability of the system was limited to a few of them.

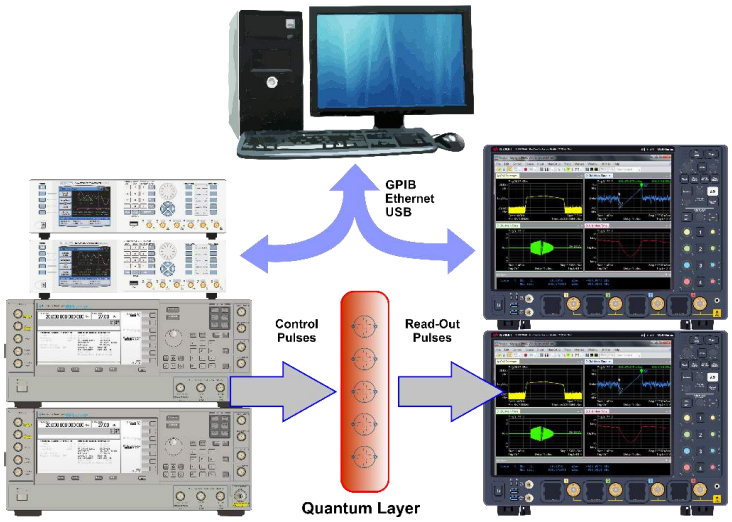
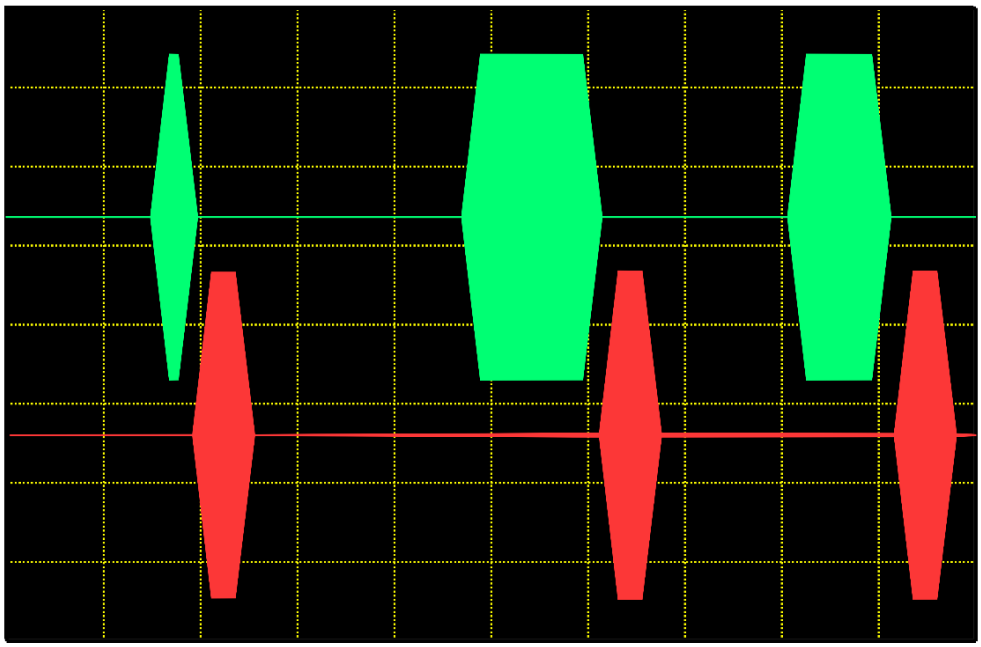


Figure 1: T&M equipment have been extensively used to control and measure Qubits in experimental QC systems. Traditional Rack&Stack instrumentation is the most popular given the level of performance and flexibility. In these experimental systems, multiple multichannel AWGs combined with additional IQ modulators and mixers are applied to the quantum layer, while Vector Spectrum Analyzers or high-bandwidth real-time digital oscilloscopes are used to read the state of the Qubits. Very complex and fast sequences of stimuli and responses can be executed thanks to the powerful triggering and sequencing capabilities of modern instruments. However, the genuine real-time close-loop control required for actual, practical quantum computing cannot be implemented given the speed limitations of the control system and the communication buses.

a) Rabi Oscillation



b) Spin Echo

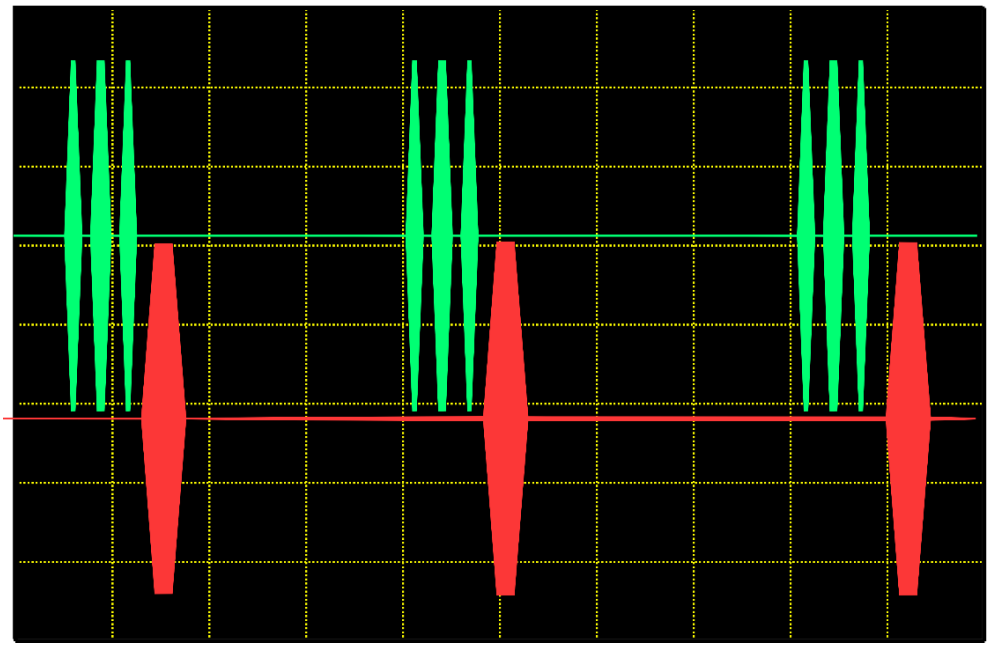


Figure 2: The way the quantum state of qubits can be controlled and captured is different for each technology and implementation. Here, two different sets of control (green) and read-out (red) RF pulses are shown for two different qubit technologies: Rabi Oscillation (a) and Spin Echo (b). They share some characteristics, though. The shape, timing, RF/μW carrier frequency and phase must be tightly controlled and may be different for each step and each pulse. Generating this kind of signals using traditional AWGs would require 4 or more channel per qubit in addition to several external IQ modulators and mixers. In real quantum computing systems, the characteristics (shape, timing) of the control pulses for each step depend on the states read after the execution of the current state and it must be analyzed and set in a matter of hundreds of ns or a few μs.

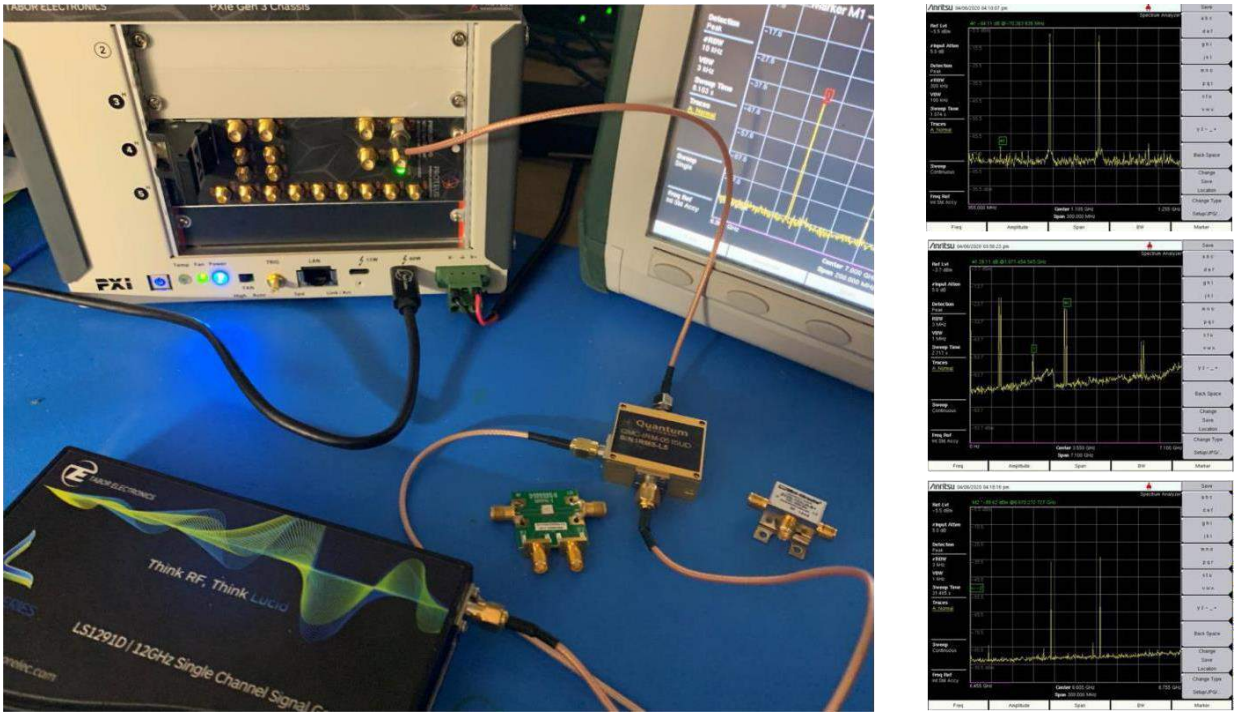


Figure 3: The traditional approach to generate RF pulses fusing an AWG is either by generating the (I/Q) baseband signals and an additional I/Q modulator, or by generating a modulated IF signal and then upconvert it to the final frequency by using a mixer. Here a Tabor Proteus P9082M, 2-channel, 9GSa/s AWG is being used to generate 2 tones around 6GHz and a mixer (shown connected) or an IQ modulator (the 4-port module at the left of the mixer). A Tabor LS1291D 12GHz analog RF signal generator is used as the L.O. required for the mixer and the I/Q modulator. Results can be seen in the column on the right. The SA capture in the center corresponds to the I/Q modulator which requires two AWG channels. The unwanted tone in the middle of the two wanted tones results from a typical impairment in IQ modulators, carrier feed-through. There are many other impairments and aligning IQ modulators is difficult and time consuming. The capture at the bottom corresponds to the same signal using an IF generated by one channel. In this case, the IF carrier frequency is around 1GHz (shown at the top capture). As the modulation of the IF carrier has been performed numerically using a single channel, there are no impairments caused by the modulation process itself and, therefore, no carrier feedthrough is visible in the Spectrum. With this particular AWG, the carrier frequency could be set to 6GHz directly so the mixer could be made redundant. (Photo and measurements courtesy of Mark Elo, Tabor Electronics, and Charles Greenberg, Astronics).

The main reason why actual computing was not possible through this kind of “scenario-oriented” approach was the speed required to perform a significant number of “feed-back/ forward” cycles in the available coherence time (survival period of superposition and entanglement for the Qubits in the system). This is especially critical for superconducting qubits where coherence time may be just a few hundreds of microseconds. This requirement results in the need to be capable of performing a single “feedback/forward” cycle in a period ranging from a few hundreds of nanoseconds up to a few microseconds. These speed requirements cannot be handled in real-time by traditional T&M instrumentation and the associated classical computing control systems. Instead, in those systems, the sequence of quantum states is predefined so AWGs apply sequentially the corresponding control and read-out signals while DSOs and digitizers capture the resulting quantum states of the qubits so their correctness and reliability can be established. In a real quantum computer, the next quantum state of the qubits depends on their previous quantum states according to the quantum gates applied

sequentially according to the quantum algorithm being executed. In order to fulfill this requirement at speeds compatible with the actual coherence time supported by the qubit technology being used, a very fast closed-loop control system, capable of reading the quantum states from the different qubits, applies the quantum gates for the current step in the algorithm, and sets the new states for all the qubits in the quantum computer (figure 4). Given the number of qubits involved in working quantum computer and the number of signals to handle, it is virtually impossible to implement such classical to quantum computing interface using traditional T&M equipment under the control of a single computer. These speed (and reasonable cost) requirements can be only met by implementing a distributed real-time closed-loop control system based totally or partially in hardware tightly connected to the waveform generation and capture blocks. Under this scheme, an FPGA or ASIC connected to high-speed DACs and ADCs controls one or a few qubits while it communicates at high speed with the other closed-loop control blocks in the system.

ny quantum bit control system is extremely sensitive to noise. In addition to traditional thermal noise, crosstalk or quantization error, any deviation of the waveforms applied to or read from qubits respect to the ideal ones can look as noise added to the system. Noise will result in higher computational errors or even system decoherence. Linear and non-linear distortions added by the signal generation and capture chains result in such deviation, thus increasing noise. System characterization, calibration and correction is paramount for a successful implementation.

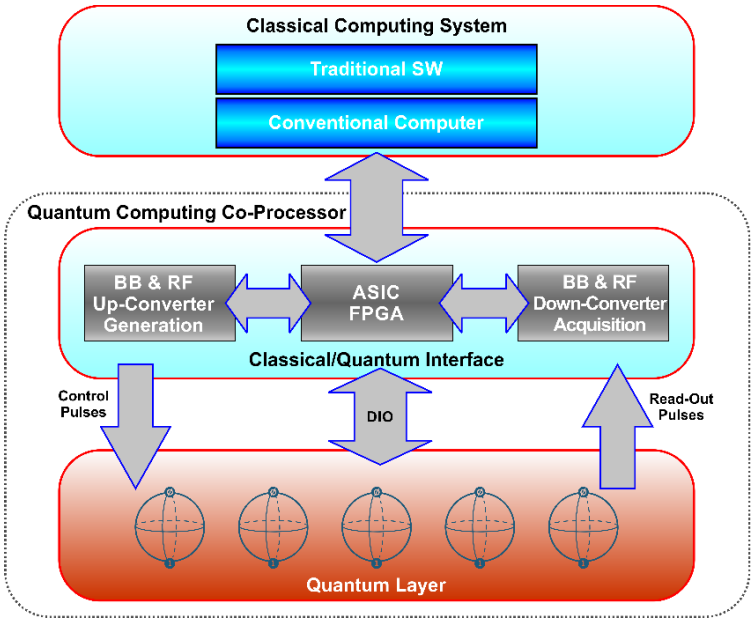


Figure 4: Operating Quantum Computing systems can be described as a classical computer connected to a quantum computing coprocessor through a Classical/Quantum interfacing block. This block must implement multiple analog (both baseband and RF) and digital input and output channels and it must take control of the feedback-forward cycles according to the quantum algorithm being executed. As the processing speed requirements are high and the processing power required grows with the number of Qubits, the ideal implementation should incorporate multiple fast signals processors in the loop. In this way, the classical computer only set-up the computing sequence, monitors the execution of the algorithm, and reads and validates results. Using specific, scalable HW in the control loop is the best way to reach the level of performance required and this is possible through the usage of application-specific IC (ASIC) or field- programmable gate arrays (FPGA). The Proteus series of Arbitrary Waveform Transceiver implements
Quantum Interface by providing all the blocks shown and incorporating an FPGA fully accessible to users.

The new Proteus platform from Tabor Electronics. Designed for Quantum Computing

During the past years, Tabor Electronics has been one of the leading suppliers of high-performance AWGs for the Quantum Computing research community. In particular, the SE5082 AWG (figure 5), with its two 5GSa/s channels and extremely high analog BW, special RF working modes to efficiently produce signals in the second and third Nyquist bands and advanced sequencing, has been extensively used in the field of Quantum Computing research. The size and cost per channel of the SE5082 makes it extremely attractive for QC researchers to be applied to “proof-of-concept” research devices.

Figure 5: The Tabor SE5082, 2-channel, 5GSa/s AWG have been used extensively in the quantum computing application area. It is ideal to generate IF and RF signals directly as its analog BW and different DAC operating modes allow for the generation of complex modulated RF signals in the second and third Nyquist band, well beyond 7GHz.

Tabor Electronics has gathered all the feed-back from QC users to define the next generation of products: the Proteus family of AWG and AWT (Arbitrary Waveform Transceiver, figure 6). Available in different form factors (PXI modular, desktop, and benchtop) and sampling rates (1.25GSa/s, 2.5Gsa/s and 9Gsa/s) with a usable analog BW close to 8GHz, all the components of the family share the same basic compact, high-density architecture, offering up to 4 16-bit AWG channels in one 2-slot PXI module or up to 12 AWG channels in a single desktop or benchtop system. Waveform memory size is huge (up to 16GSamples) and memory segmentation and advanced sequencing (including conditional branching) can support the most extreme synchronized waveform generation scenarios.

However, although impressive, the AWG performance is not the only appealing characteristic of the Proteus solution for quantum computer researchers and designers. It is the built-in capability of closing the loop and implement “feedback-forward” cycles at the right speed what allows operational quantum computers to work. And this is possible for two reasons. First, the Proteus family creates a new product category, the AWT (Arbitrary Waveform Transceiver), by incorporating a two-channel 12-bit digitizer per PXI module (up to 4 channels per desktop or benchtop system) running at up to 5.4GSa/s with enough analog BW to digitize signals up to 9GHz. The second reason is the availability of a high-speed FPGA (Xilinx UltraScale KU-060) that is open for users to be programmed. This FPGA is directly connected to the analog outputs (AWG) and inputs (digitizer), the DDR4 massive memory, multiple digital 1.25 Gbps digital input/outputs (8 markers and 2 GPIO) and the PCIe Gen3, 8-lanes backplane capable of supporting sustained communication at 50Gb/s (figure 7).

a)

b)

Figure 6: The new Tabor Proteus series of Arbitrary Waveform Transceivers is designed to match the requirements of Quantum Computer designers. It combines analog and digital high-speed inputs and outputs in the same platform along with a user-accessible FPGA for applications required closed-loop and real-time signal processing. The PXI modules (a) can incorporate up to 4 channels of AWG (1.25, 2.5, or 9GSa/s) and 2 digitizer channels (2.7 or 5.4 GSa/s) with up to 10 digital input/outputs (1.25gbps) in a single 2 or 3-slot PXI module. The benchtop models (b) can incorporate up to 12 channels of AWG and up to 4 digitizer channels in a single device. Multiple modules and devices can operate synchronously without the need for additional synchronization hardware.

Both the AWG and digitizer blocks have been designed to directly generate and capture RF and microwave signals. Analog output channels incorporate internal numerical IQ modulators and up converters (DUC) while analog input channels can incorporate digital down converters and demodulators as standard processing blocks in the FPGA. RFquality of the signals in excellent regarding SFDR and phase noise.

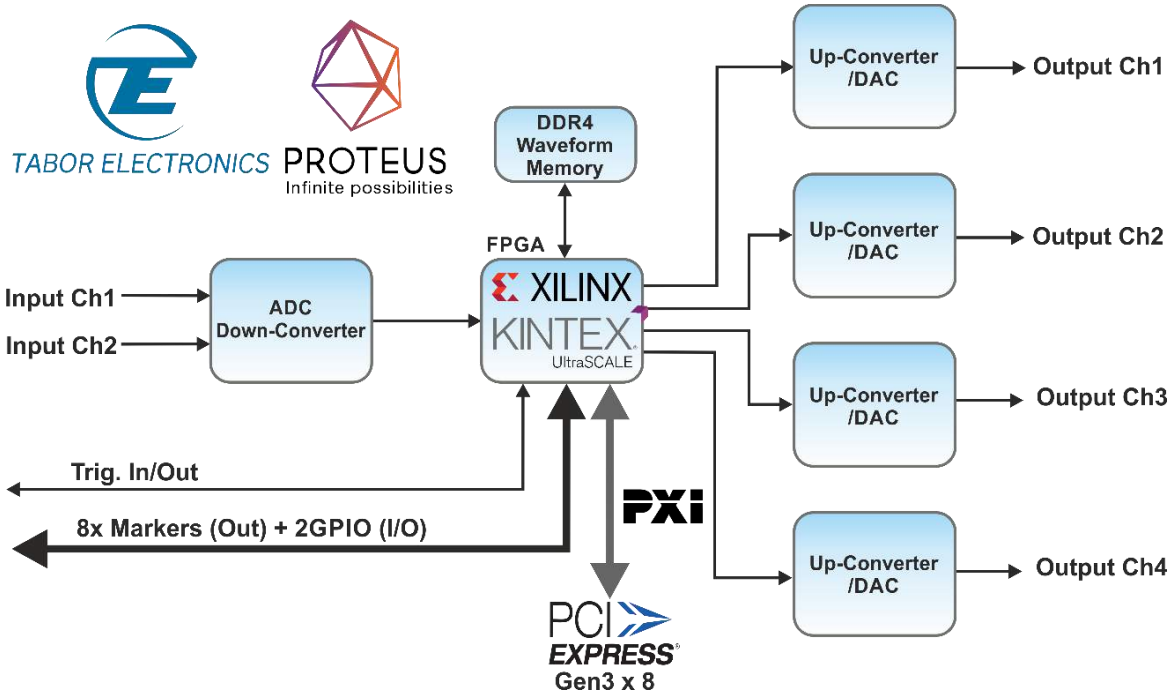


Figure 7: The block diagram for a Proteus PXI AWT module is very similar to the one for the Classical/Quantum Computing Interface shown in figure 4. Both the inputs and outputs can be used to the acquisition and generation of baseband (DC to Sample Rate /2) and RF over multiple Nyquist Bands up to 8GHz. A great portion of the gates in the Xilinx Kintex© FPGA are free to use so any application-specific closed loop control and/or signal processing application can be implemented. The massive DDR4 memory is capable of storing up to 16GSamples while the PCIe Gen.3, 8 lanes bus can handle continuous streaming from the digitizer or to the AWG at sampling rates beyond 6GSa/s. The same bus allows for the fast interconnection of multiple modules.

Direct to Microwave signal generation and acquisition

The generation of complex RF signals requires the simultaneous control of both the amplitude and phase of a carrier. One way to implement such control is an IQ modulator (figure 8a, left). There, the magnitude and phase instantaneous states are converted into a baseband complex modulating signals where the real part (or In-phase, I) modulates the amplitude of a carrier while the imaginary component (or quadrature, Q) controls the amplitude of an orthogonal (pi/2 phase) version of the same carrier before being added together. In traditional VSGs (Vector Signal Generators), an internal or external 2-channel AWG produces the baseband I/Q waveforms applied to the IQ modulator while an internal synthesizer produces the two orthogonal CW carriers applied to the I and Q modulators. Under this scheme, the sampling rate of the AWGs does not depend on the carrier frequency but on the modulation BW (Figure 8a, right). Basically, sample rate for the AWGs must be equal or higher than the modulation bandwidth as the modulation bandwidth of a quadrature modulator is twice the bandwidth of the I and Q baseband signals. The accuracy and alignment of all the building blocks is extremely important, and their importance grows with the modulation bandwidth. Any difference in amplitude,

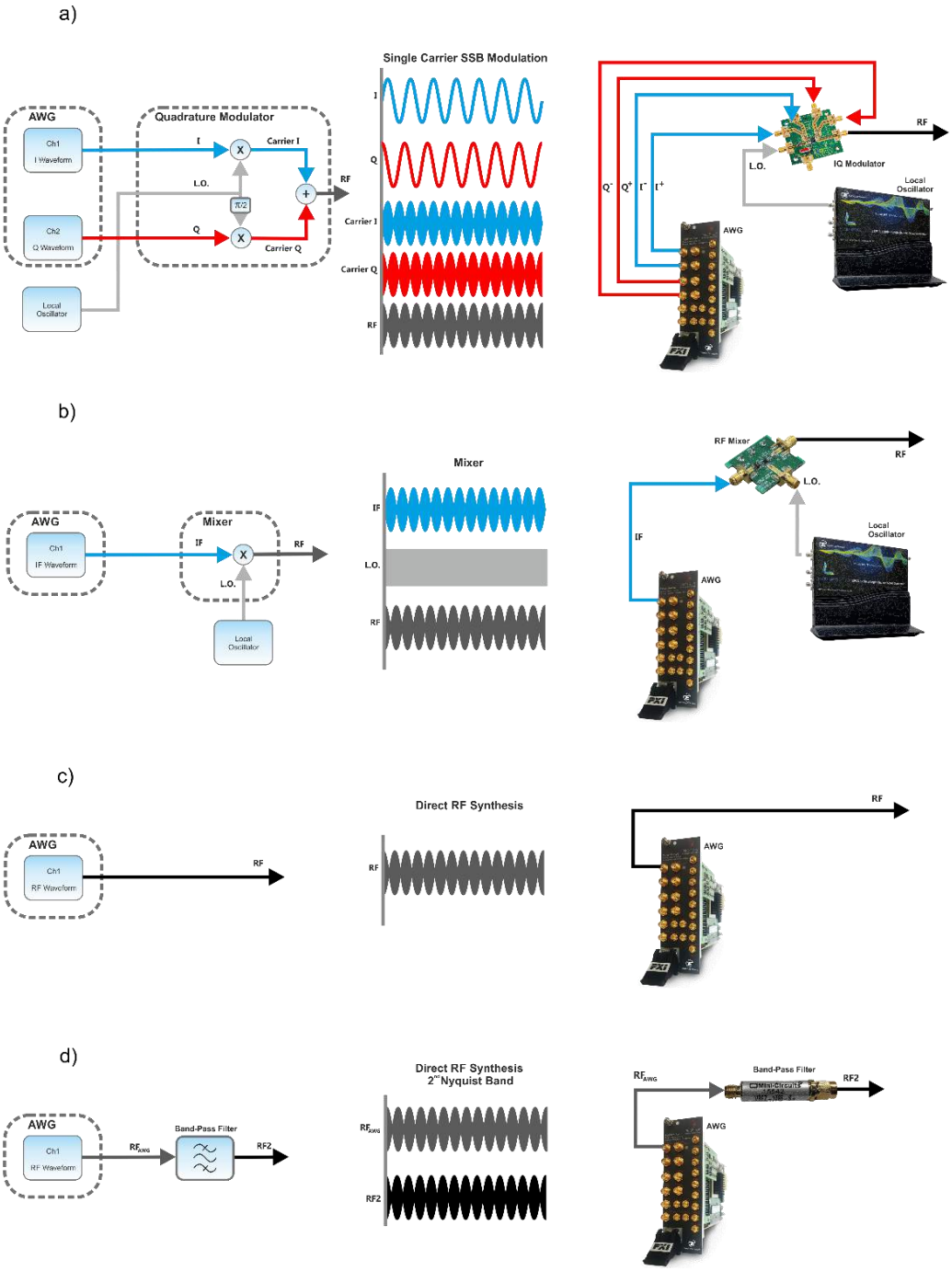


Figure 8: AWGs have been always part of any vector signal generation system as an internal or external component. In a) the traditional IW generation scheme is shown. Two channels are used to generate the I and Q components to feed an IQ modulator. The required sampling rate for the AWG depends on the modulation bandwidth, not in the carrier frequency. In b), a single channel AWG is used to generate a modulated IF signal to feed a mixer. The mixer up converts the IF signal to the final frequency. In this case, sampling rate is mainly determined by the IF carrier frequency. In both cases an additional L.O. source is required.
When sampling rate is enough (at least twice the carrier frequency) the final RF signal can be generated directly as seen in c) without the need for any external mixer, modulator or L.O: source. It is even possible to generate RF signals beyond the Nyquist frequency by using images of the signal located in higher order Nyquist bands as seen in d). Usually, a BPF is required to get rid of the unwanted images.

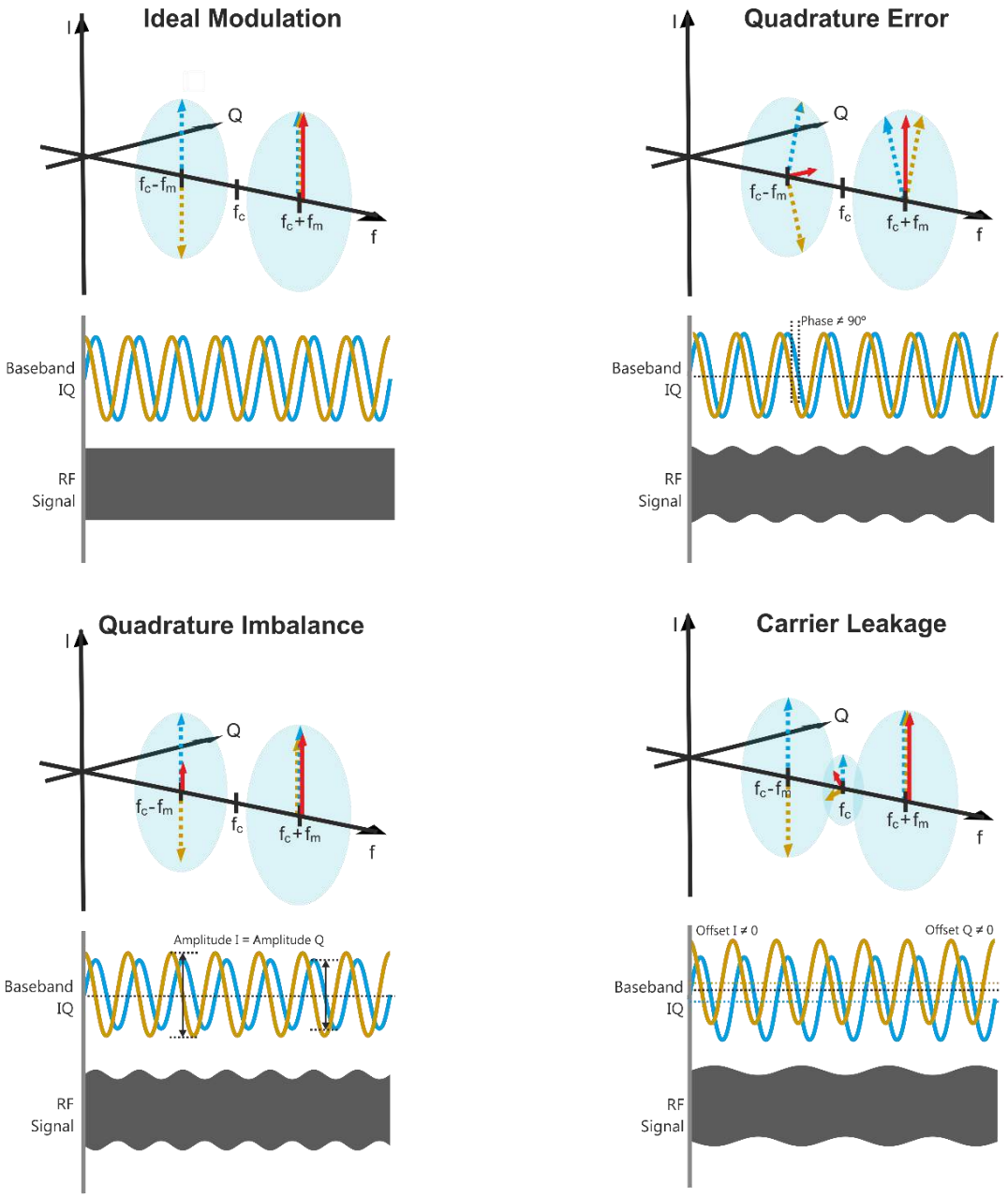


Figure 9: I/Q modulation is very sensitive to any inaccuracy affecting the I and Q components and the orthogonal fc carriers applied to them. A good way to visualize the influence of these inaccuracies is by applying two fm sinewaves with a 90^{O} phase difference. In a perfect situation, the modulated I and Q components are added together in one of the fc±fm sidebands and canceled in the other (top left). If amplitudes of the I and Q components are not the equal, cancellation is not perfect, and the Quadrature Imbalance impairment shows up (bottom left). If relative phase for carriers are not accurate, an unwanted residual sinewave shows-up resulting in the Quadrature Error impairment (top right). Finally, if some DC component is added to any of the modulating sinewaves or carriers, an unwanted residual carrier will appear (bottom right). This impairment is known as Carrier Leakage. In the real world there may be some other linear and non- linear impairments with similar effects. As any complex-modulated signal can be seen as the addition of infinite sinusoids, these impairments result in the signal interfering itself and reducing the signal-to-noise ratio. Identifying and measuring these impairments independently is necessary to apply corrections to reduce them. This can be quite difficult and time-consuming to do. Numerical quadrature modulation does not suffer this problem as all the components behave ideally.

frequency response, skew, sampling clock phase noise, etc. in the AWG will show up as a degraded quality RF signal. The same is true for the IQ modulator itself including the orthogonality of both carriers. It also applies to the L.O. synthesizer. All the linear or non-linear distortions can be measured through a single metrics such as the EVM (error vector magnitude), very popular in the wireless communication environment (figure 9).

Another way to generate RF modulated waveforms is by using an AWG to produce a fully modulated IF signal with one single channel and then upconvert it to the final carrier frequency using an external mixer (figure 8b). This scheme requires an additional CW L.O. to feed the mixer. The advantage of this architecture is that the IQ modulation of the IF carrier is performed numerically when the waveform is calculated. As a result, there will not be I/Q alignment errors (amplitude, frequency response, skew, quadrature). The requirements for sampling rate will be higher, though. Sampling rate will have to be, at least, twice the maximum frequency component of the IF waveform. This means that the sampling frequency must be always higher than twice the carrier frequency and the modulation bandwidth.

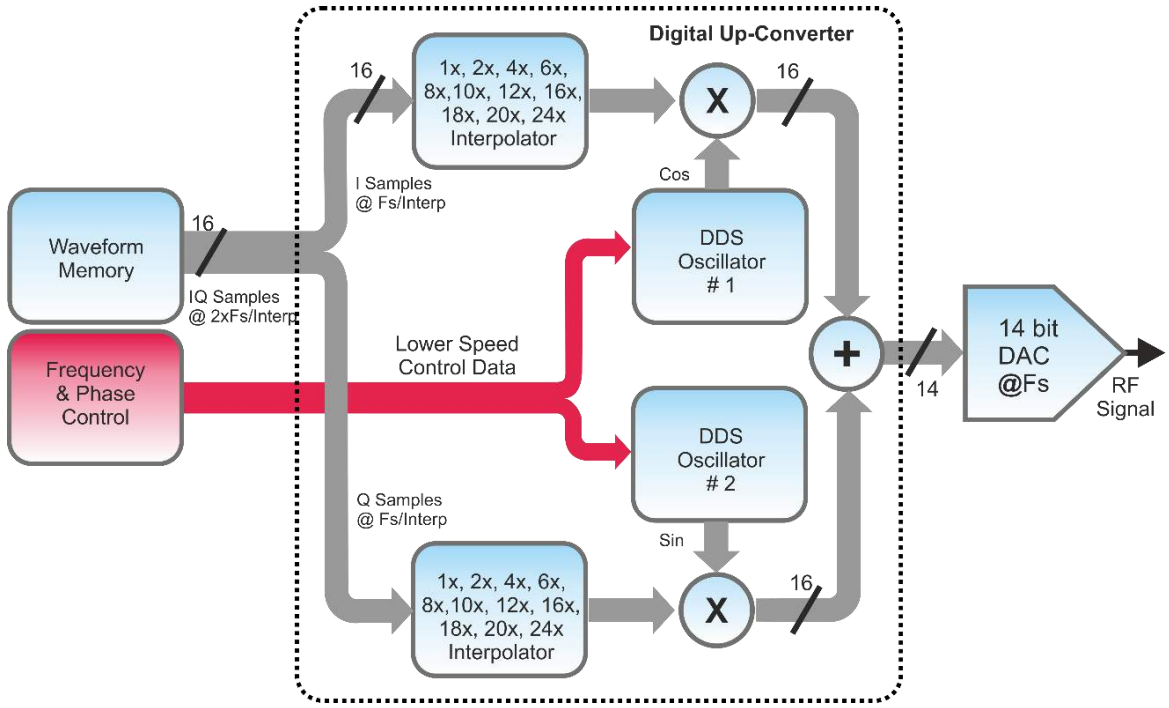


Figure 10: Any AWG can generate complex modulated IF/RF signals by just calculating the complete, modulated waveform and transferring it to the waveform memory. The sampling rate for the calculated and the generated waveforms will be the same and it is related to the carrier frequency. A different approach is implementing in hardware a digital up-converter or DUC (here, a block diagram of the DUC implemented for each DAC in the Proteus series). The most important advantage consists in the fact that the waveform memory will store complex sample pairs (I/Q) that will be demultiplexed internally to two different multipliers where they will be combined with two orthogonal carriers generated by two NCOs set at the same frequency (fc) and 90^{O} differential phase. As the I and Q waveforms are not related with the carrier frequency, these waveforms can be sampled at a sampling rate enough for the modulation bandwidth (basically sample rate >= modulation bandwidth). In order to match output sampling rate and the baseband waveforms sampling rate, an additional interpolation block must be added. In real DACs, interpolating factors are limited to a set of integer values so there is an integer relationship between the input and the output sampling rates. This scheme has several advantages as memory and calculation time is saved and the fc can be changed without having to recalculate the waveform, even on the fly.

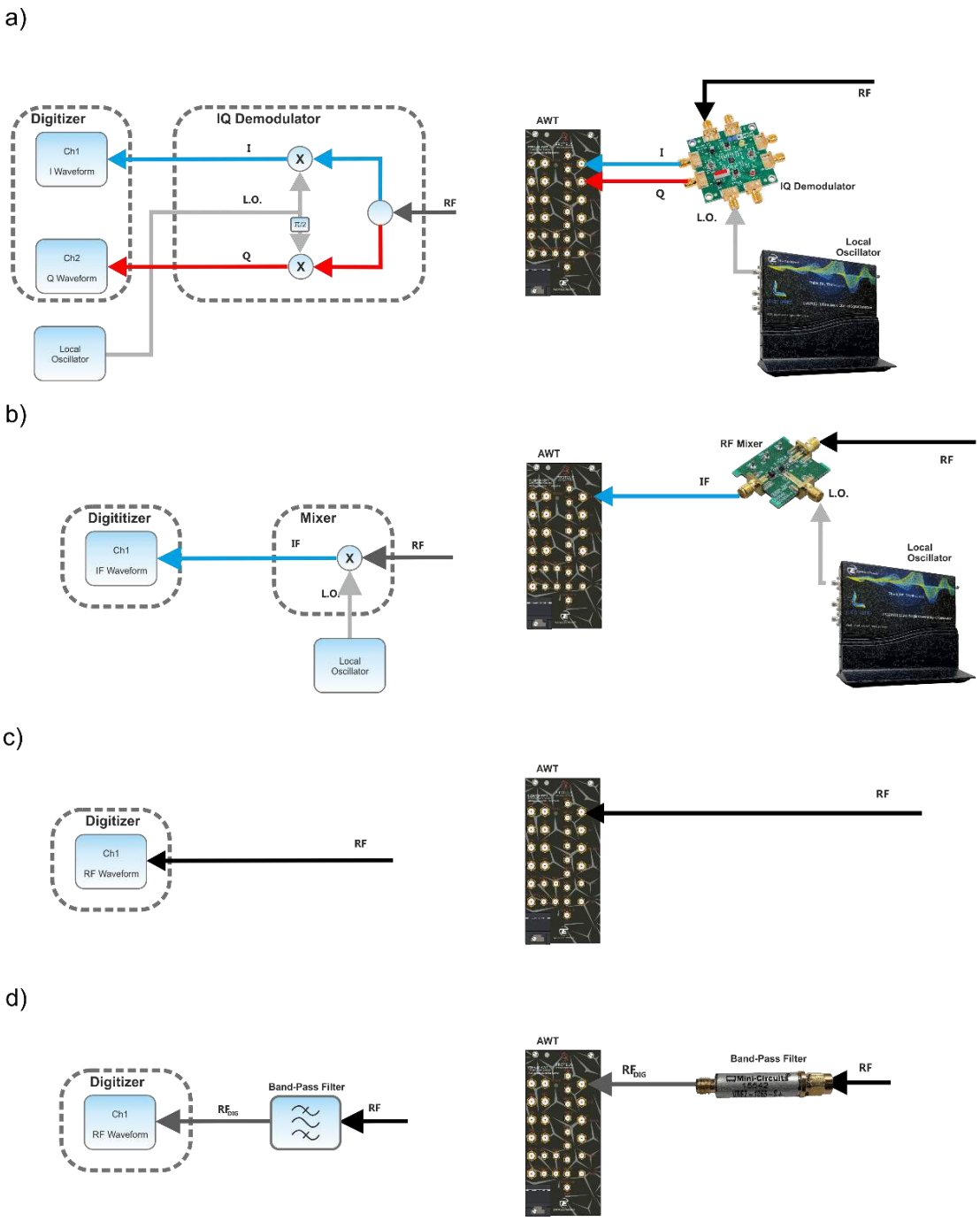


Figure 11: The capture of RF signals using a digitizer is quite symmetrical to the way an AWG generates them with the signal flow going in the opposite direction. An external IQ demodulator can feed two digitizer channels (a), or a mixer can generate an IF signal at a lower frequency that can be digitized using one channel (b). If sampling rate and analog BW are enough, the RF signal can be directly captured in the first Nyquist band of the digitizer (c) or in a higher order Nyquist band by undersampling (d). In this case a BPF must be used to remove any signal located in the other Nyquist bands, if any.

Eventually, if the sampling rate of the AWG is high enough, a modulated RF carrier can be generated directly (figure 8c). In this case, the requirements for the sampling rate will be even higher as the final carrier frequency will be higher than any IF frequency. It is true that ENoB (Effective Number of Bits) decreases as sampling rate grows, but the resulting quantization noise is spread over a wider BW, so the noise power density does not grow that much. When sampling rate is not enough for the target carrier frequency, an image located in a higher order Nyquist band can be used instead if the analog BW allows (figure 8d). AWGs such as the SE5082 incorporate DAC modes (RF mode) designed to minimize the amplitude of the image in the first Nyquist Band and emphasize the images in the second and third Nyquist band. Typically, a BPF is connected at the output to get rid of the undesired images. The main advantage of this RF generation scheme is the simplicity of it as no external devices (i.e. mixers, modulators, or L.O. sources) are necessary.

IF/RF direct generation requires higher sampling rates but less channels than baseband generation. It also requires higher sampling rates, and a higher sampling rate results in a larger waveform memory if the same time window must be generated. In order to ease those requirements, some RF-oriented AWGs, such as the Proteus family, incorporate an internal real-time I/Q modulator or DUC (Digital Up- Converter, figure 10). The beauty of real-time I/Q modulation is that it is associated to an ideal interpolation block so the I/Q sample pairs (now stored together and interleaved in the same waveform memory) are fed to the DAC block at a much lower sampling rate, defined by the modulation BW, so waveform memory and calculation and transfer time is greatly reduced. Additionally, the carrier frequency can be changed without modifying the I/Q waveform, just by setting the NCOs to the new frequency.

The same basic architectures can be also applied to the acquisition of modulated RF signals using DSOs or digitizers (figure 11). In particular, it is possible to directly capture an RF signal even beyond the first Nyquist band by under sampling the input signal if the analog BW of the digitizer is high enough. In order to do so, the center of the useful Nyquist band must be aligned with the RF signal to be captured by setting the appropriate sampling rate (figure 12a). Doing so, the waveform will show up as an image in the first Nyquist band. Depending on the Nyquist band being used, the spectrum of the image signal in the first Nyquist band will be reversed. Any other signal in any other Nyquist band will interfere with the target signal, so it may be necessary to apply a BPF to the input. The waveform can then be stored in the acquisition memory and further processed afterwards. Sampling rate and memory requirements for the acquisition are linked to the ADC sampling rate. However, the digitizer waveform could be processed in real-time through a DDC (Digital Down-Converter, an I/Q demodulator, figure 12b) to I/Q baseband and decimated so the final sampling rate is equal or higher than the modulation BW and not set by the carrier frequency. This operation also results in a “processing gain” (in effective bits) caused by the original oversampling respect to the one after decimation. A lower sampling rate results in lower waveform memory requirements and, even more importantly, faster waveform processing, a critical need for closed loop control.

The AWG section of the Proteus family is a good example of a direct-to-RF arbitrary waveform generation. All the Proteus models share the same DAC platform. However, the 1.25GSa/s and 2.5GSa/s maximum sample rate models can work in the 16-bit mode only. The 9GSa/s mode can still work in the 16-bit mode up to 2.5GSa/s but an additional working mode extends the sampling rate in direct conversion to 9GSa/s with 8-bit samples. Additionally, the 16-bit mode combined with the built-in real- time interpolation and DUC, allows for the generation of RF waveforms up to 7.5GHz (first and second Nyquist band) with high-resolution waveforms

and excellent dynamic range and modulation bandwidth (>2GHz). Higher modulation bandwidths (>4GHz) can be still reached through the 8-bit mode. One of output stage options is especially designed for higher performance RF and μW signal generation. It removes any amplifier from the signal path, so linearity and bandwidth are improved. Additionally, it is AC-coupled as many RF devices are very sensitive to any remaining DC offset. SFDR (Spurious-Free Dynamic Range) specification offered by this option is excellent and can be >80dB over the full usable BW and even >90dB in the 1-2GHz range.

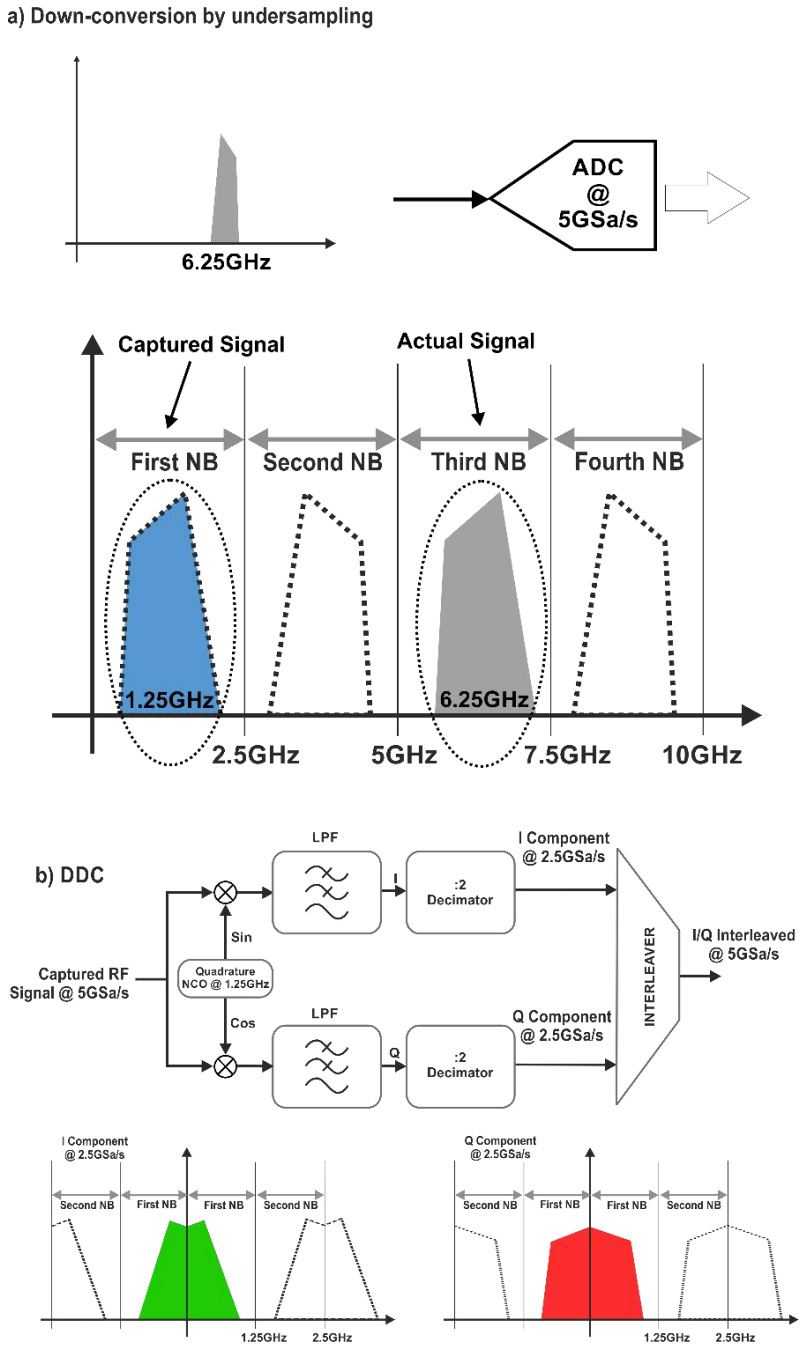


Figure 12: In order to store and process an RF signal captured by a digitizer, it must be properly digitized. Waveforms captured by any ADC can be modelled as waveforms located in the first Nyquist band (DC-SR/2).

When the analog BW of the ADC and the aperture time of the S/H circuit is small, any waveform fitting completely in any of the Nyquist band below the analog BW of the digitizer can be successfully captured as it was down-converted (a). Depending on the Nyquist band being used, the captured waveform will be reversed in the frequency domain. Any BW-limited signal in the first Nyquist band can be down-converted to complex baseband components (IQ) by applying a DDC (Digital Down Converter). Again, the DDC block diagram is very similar to a DUC with the signals flowing in the opposite direction. Sampling rate can be reduced (by decimation) according to the modulation bandwidth of the signal. Reducing the sampling rate improves waveform storage requirements and signal processing. The above example shows how a 6.25GHz signal can be captured by a 5GSa/s digitizer with more than 2GHz Analysis Bandwidth

The Proteus DUC is a very flexible and powerful one. The DUC can be combined with the built-in interpolator so the waveform sampling rate can be adapted to the modulation BW rather than the carrier frequency. Interpolation factors supported are 2X, 4X, 6X, 8X, 10X, 12X, 16X, 18X, 20X, and 24X (fig. 13a). Such flexible choice allows for an optimal effective sampling rate selection and the corresponding waveform memory savings. Interpolation, to be useful, must be combined with the application of a high-quality interpolation low-pass filter. The digital interpolation filters applied for every interpolation factor are excellent and show a 0.01dB ripple in the passband BW (0.4 X input waveform sampling rate) and a stopband attenuation higher than 90dB (fig. 13b). NCOs are a very basic component of any DUC. Two NCOs working as a single quadrature oscillator are required for IQ modulation. The Proteus internal architecture allows for independent control of both frequency and phase for each 48-bit NCO in the IQ modulator. For regular IQ modulation, both NCOs share the same frequency while phase difference is set to 90^{o}. Relative phase control is also possible between multiple channels in the same or multiple Proteus modules. This characteristic is paramount in any multiple RF channel generation application where carrier coherence is required. Phase-array radar, MIMO, and Qubit control are just some of these application areas.

The Proteus AWT digitizer section can work in two modes. In the basic mode all the channels can work up to 2.7GSa/s with 12 bits of vertical resolution. In the fast mode, every two channels can be combined to offer 5.4GSa/s sampling rate. Besides being usable as a regular digitizer from DC up to SR/2, it has been designed to be used as an IF/RF/ μW acquisition system. Analog BW is excellent (>8GHz), and it can acquire bandwidth-limited signals (i.e. modulated carriers) in the second, third, and even the fourth Nyquist band. Supported modulation BW can reach > 1.3GHz for the basic mode and over 2.5GHz for the fast mode. The Proteus architecture also allows the implementation of additional waveform real-time processing implemented as standard blocks in the embedded FPGA. One of the blocks implemented is a DDC (or an I/Q demodulator). The DDC results in a stream of complex, baseband IQ samples that can be filtered and decimated based in the application needs. The sampling rate reduction results in an easier later processing and acquisition memory savings. The software trigger system can also trigger the acquisition based in the RF instantaneous power or RF pulse duration. Acquisitions can incorporate pre- trigger information and multiple frame time-stamped acquisitions with extremely low dead-time are possible. Data reduction can help in speeding up signal processing and even identification.